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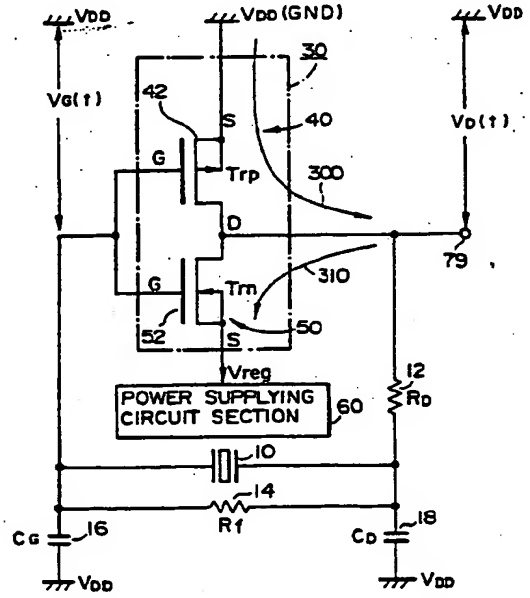
(54) Oscillation circuit, electronic circuit using the same, and semiconductor device, electronic equipment, and timepiece using the same

(57) This invention relates to a crystal oscillation circuit that oscillates stably with a low power consumption. This crystal oscillation circuit comprises an inverting amplifier, a crystal oscillator, and a feedback circuit that inverts the phase of an output from this inverting amplifier and feeds it back as an input. The sum of the absolute value of the threshold voltage of a first semiconductor switching element and the absolute value of the threshold voltage of a second semiconductor switching element is set to be greater than or equal to the absolute value of the potential difference between first and second potentials, when said inverting amplifier includes the first and second semiconductor switching elements.

FIG. 1



EP 0 851 323 A1

Descripti n

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to an oscillation circuit, an electronic circuit using that oscillation circuit, and a semiconductor device, electronic equipment, and timepiece using that oscillation circuit or electronic circuit.

Description of the Related Art

Oscillation circuits that use crystal oscillators are widely employed in the art in devices such as portable timepieces, portable telephones, and computer terminals. It is necessary to design such portable items of electronic equipment in such a manner that they are economical in their power consumption and have longer batt ry lives.

This crystal oscillation circuit comprises an inverting amplifier and a feedback circuit that is provided with a crystal oscillator. The inverting amplifier comprises a pair of transistors where the gate of each of these transistors is used as an input side and the drain thereof is used as an output side, by way of example. In this case, the drain sides of these two transistors are connected together and the source sides thereof are connected to ground and a power voltage side, respectively.

If the power voltage is applied to the inverting amplifier in the crystal oscillation circuit of this configuration, the phase of the output of the inverting amplifier is inverted through 180 degrees and the thus inverted signal is fed back to the gate of each transistor as an input. The transistors configuring the inverting amplifier are turned on and off alternately by the operation of this feedback, the oscillation output of the crystal oscillation circuit gradually increases, and thus the oscillator starts to oscillate stably.

However, the absolute value of a voltage V_{reg} applied to the inverting amplifier in this prior-art crystal oscillation circuit is set to be greater than the total of the absolute values of the threshold voltages V_{TP} and V_{TN} of the transistors in this circuit, as follows:

$$|V_{reg}| > |V_{TP}| + |V_{TN}| \quad (1)$$

The current inventors have discovered that this is the cause of a short-circuiting current I_S that flows from the high potential side to the low potential side within the inverting amplifier, which causes a problem when trying to reduce the power consumption of the entire circuit.

SUMMARY OF THE INVENTION

An objective of this invention is to reduce the above short-circuiting current that flows through the inverting amplifier and thus provide an oscillation circuit that can oscillate with a low power consumption, an electronic circuit that uses such an oscillation circuit, and a semiconductor device, electronic equipment, and timepiece that use this oscillation circuit or electronic circuit.

In order to achieve the above objective, an oscillation circuit in accordance with a first aspect of this invention comprises an inverting amplifier including a first semiconductor switching element and a second semiconductor switching element;

wherein the first and second semiconductor switching elements are prevented from being on simultaneously to limit a short-circuiting current flowing through the inverting amplifier when the first and second semiconductor switching element is driven.

This configuration makes it possible to limit the short-circuiting current flowing through the inverting amplifier, making it possible to provide an oscillation circuit that can oscillate with a low power consumption.

The sum of the absolute value of the threshold voltage of the first semiconductor switching element and the absolute value of the threshold voltage of the second semiconductor switching element may be set to be greater than or equal to the absolute value of the power voltage of the inverting amplifier, to limit a short-circuiting current flowing through the inverting amplifier.

The oscillation circuit of this invention may further comprise a feedback circuit having a crystal oscillator connected between the output and input sides of the inverting amplifier, for causing the phase of an output signal from the inverting amplifier to invert and feeding the thus inverted signal back to the inverting amplifier as an input;

wherein the inverting amplifier comprises a first circuit including the first semiconductor switching element, and a second circuit including the second semiconductor switching element;

wherein the first semiconductor switching element is connected to the side of a first potential and is driven to be turned on and off by the feedback input, to excite the crystal oscillator;

wherein the second semiconductor switching element is connected to the side of a second potential that differs from the first potential and is driven to be turned on and off by the feedback input at a timing that differs from that of the first semiconductor switching element, to excite the crystal oscillator; and

wherein the sum of the absolute value of the threshold voltage of the first semiconductor switching element and the absolute value of the threshold voltage of the second semiconductor switching element is set to be greater than or equal to the absolute value of the power voltage of the inverting amplifier, to limit a short-circuiting current flowing through the inverting amplifier.

In this case, when a voltage is applied to the inverting amplifier in the crystal oscillation circuit, excitation of the crystal oscillator starts. The phase of the output of the inverting amplifier is inverted by the feedback circuit and is fed back as an input. The operations of inverting,

amplifying, and outputting this feedback input signal by the inverting amplifier are repeated.

During this time, the first and second semiconductor switching elements that configure the inverting amplifier are driven to be turned on and off at mutually different timings by this feedback input, to excite the crystal oscillator.

As stated above, the sum of the absolute values of the threshold voltages of the first and second semiconductor switching elements can be set to be greater than or equal to the absolute value of the power voltage of the inverting amplifier. This prevents the first and second semiconductor switching elements from being driven to turn on simultaneously when the circuit is operating, and, as a result, the short-circuiting current flowing through the inverting amplifier can be greatly reduced, making it possible to reduce the power consumption.

In particular, by forming the first and second transistors in such a manner that the threshold voltage conditions are satisfied, there is no further need for means for dealing with this short-circuiting current, making it unnecessary to use special circuit components for counteracting this short-circuiting current. This makes it possible to reduce the power consumption of the crystal oscillation circuit without adversely affecting the degree of integration of the entire circuit.

Note that it is necessary to set each of the absolute values of the threshold voltages of these first and second semiconductor switching elements to be less than the absolute value of the power voltage of the inverting amplifier.

The oscillation circuit may further comprise a bias circuit for applying a first direct current bias voltage and a second direct current bias voltage to gates of the first semiconductor switching element and the second semiconductor switching element, respectively;

wherein the first and second direct current bias voltages shift the values of the direct current potentials of feedback inputs that are input from the inverting amplifier to the gates of the first and second semiconductor switching elements, to prevent the first-and second semiconductor switching elements from being on simultaneously.

The oscillation circuit may further comprise:

a feedback circuit having a crystal oscillator connected between the output and input sides of the inverting amplifier, for causing the phase of an output signal from the inverting amplifier to invert and feeding the thus inverted signal back to the inverting amplifier as an input; and

a bias circuit for applying a direct current bias voltage to the inverting amplifier;

wherein the inverting amplifier comprises:

a first circuit connected to the side of a first potential and comprising the first semiconductor switching element; and

a second circuit connected to the side of a second potential that differs from the first potential and comprising the second semiconductor switching element;

wherein the first semiconductor switching element is connected to the side of the first potential and is driven to be turned on and off by the feedback input that is input to a gate, to excite the crystal oscillator;

wherein the second semiconductor switching element is connected to the side of the second potential and is driven to be turned on and off by the feedback input that is input to a gate at a timing that differs from that of the first semiconductor switching element, to excite the crystal oscillator;

wherein the bias circuit comprises:

a first bias circuit for applying a first direct current bias voltage to the gate of the first semiconductor switching element; and

a second bias circuit for applying a second direct current bias voltage to the gate of the second semiconductor switching element; and

wherein the first and second direct current bias voltages shift the values of the direct current potentials of feedback inputs that are input from the inverting amplifier to the gates of the first and second semiconductor switching elements, to prevent the first and second semiconductor switching elements from being on simultaneously.

By employing the above configuration, there is no common-on time at which both of the first and second semiconductor switching elements are on, while the first and second semiconductor switching elements that configure the inverting amplifier are driven to be turned on and off at mutually different timings by this feedback input, to excite the crystal oscillator. Therefore the short-circuiting current flowing through the inverting amplifier can be greatly reduced, making it possible to achieve a crystal oscillation circuit that can oscillate stably at a low power consumption.

In particular, the short-circuiting current of the inverting amplifier can be reduced, even when the absolute values of the threshold voltages of the first and second semiconductor switching elements are made small. The power voltage of the crystal oscillation circuit can therefore be reduced by that amount, making it possible to reduce the power consumption of the oscillation circuit even further.

In this case, the first direct current bias voltage may be set to the first potential and the second direct current bias voltage may be set to the second potential.

The direct current potentials of the inputs fed back

to the gates of the first and second semiconductor switching elements can be shifted towards the respective first and second potential sides of the power source by the application of the thus-set direct current bias voltages. This makes it possible to provide a crystal oscillation circuit which has a simple circuit configuration and which can reduce the short-circuiting current of the inverting amplifier.

The first and second semiconductor switching elements may be configured by using field-effect transistor elements of differing conductivity types.

According to a second aspect of this invention, there is provided an electronic circuit comprising the above oscillation circuit of this invention.

Similarly, according to a third aspect of this invention, there is provided a semiconductor device comprising one of the above oscillation circuit and the electronic circuit of this invention.

Furthermore, according to a fourth aspect of this invention, there is provided electronic equipment comprising one of the above oscillation circuit and the electronic circuit of this invention.

This can reduce the power consumption of an item of portable electronic equipment, such as a portable telephone or computer terminal, and thus makes it possible to reduce the consumption thereof of power from an internal battery or secondary battery.

Finally, according to a fifth aspect of this invention, there is provided a timepiece comprising one of the above oscillation circuit and the electronic circuit of this invention.

This makes it possible to implement a portable timepiece that has a low power consumption, which enables the design of a timepiece that is itself smaller and uses an even smaller battery. Alternatively, the battery life thereof could be extended even when a battery of the same capacity is used.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram of a first embodiment of the crystal oscillation circuit in accordance with this invention;

Fig. 2 is a timing chart of a prior-art circuit;

Fig. 3 is a timing chart of the circuit of Fig. 1;

Fig. 4 is a illustrative drawing of the relationship between the threshold voltages, the power source potential, and the ground potential of the prior-art circuit;

Fig. 5 is a illustrative drawing of the relationship between the threshold voltages, the power source potential, and the ground potential of the first embodiment;

Fig. 6 is a graph of the V_{GS}-I_D characteristic of an enhancement-mode transistor;

Fig. 7 is a circuit diagram of a second embodiment of the crystal oscillation circuit in accordance with this invention;

Fig. 8 is a timing chart of the second embodiment;

Fig. 9 is a circuit diagram of another crystal oscillation circuit;

Fig. 10 is a timing chart of the circuit of Fig. 9;

Fig. 11 is a timing chart of a variation;

Fig. 12 is a circuit diagram of yet another crystal oscillation circuit;

Fig. 13 is a timing chart of the circuit of Fig. 12;

Fig. 14 is a timing chart of a variation;

Fig. 15 shows a variation on the crystal oscillation circuit of Fig. 9;

Fig. 16 is a circuit diagram of a variation on the inverting amplifier in the crystal oscillation circuit of Fig. 12; and

Fig. 17 is a circuit diagram of another variation on the inverting amplifier in the crystal oscillation circuit of Fig. 12;

DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of this invention will be described below with reference to the accompanying drawings.

First Embodiment

A crystal oscillation circuit relating to a first embodiment of this invention is shown in Fig. 1. The crystal oscillation circuit of this embodiment is one that is used in a quartz wristwatch.

This crystal oscillation circuit comprises an inverting amplifier 30 and a feedback circuit. This feedback circuit comprises a crystal oscillator 10, a resistor 14, and phase-compensation capacitors 16 and 18. It inverts the phase of an output $V_{D(t)}$ of the inverting amplifier 30 by 180 degrees and inputs the inverted signal as a gate signal $V_{G(t)}$ to the gate of the inverting amplifier 30 as feedback.

The configuration of the inverting amplifier 30 is such that it is connected between a first potential side and a second potential side that is at a lower potential, and it is powered by the potential difference between

these two potentials. In this particular case, the first potential is set to the ground potential V_{DD} and the second potential is set to a negative power source potential V_{reg} that is supplied from a power supplying circuit section 60.

The inverting amplifier 30 comprises a first circuit 40 and a second circuit 50.

The first circuit 40 comprises a p-type field-effect transistor 42 that functions as a first semiconductor switching element. The source of this transistor 42 is connected to ground, the drain thereof is connected to an output terminal 79 side, and the feedback signal $V_{G(t)}$ is applied to the gate thereof.

The second circuit 50 comprises an n-type field-effect transistor 52 that functions as a second semiconductor switching element. The source of this transistor 52 is connected to the power source terminal side of the power supplying circuit section 60, the drain thereof is connected to the output terminal 79 side (in this case, it is actually connected to the drain of the transistor 42), and the feedback signal $V_{G(t)}$ is applied to the gate thereof.

A transistor that is both a p-type as well as an enhancement-mode field-effect transistor is used as the transistor 42, and a transistor that is both an n-type as well as an enhancement-mode field-effect transistor is used as the transistor 52. The values of the threshold voltage V_{TP} of the transistor 42 and the threshold voltage V_{TN} of the transistor 52 are such that the total absolute value thereof is greater than or equal to the absolute value of the power voltage applied to the inverting amplifier 30 (in this embodiment, the power voltage is V_{reg}, which is the potential difference between the ground potential and the power source potential, because the ground potential V_{DD} is set to zero), as given by the following equation:

$$|V_{reg}| \leq |V_{TP}| + |V_{TN}| \quad (2)$$

In addition, the absolute values of the threshold voltages of the transistors 42 and 52 are each set to be less than the absolute value of the power voltage, as follows:

$$|V_{reg}| > |V_{TP}| \quad (3)$$

$$|V_{reg}| > |V_{TN}|$$

This ensures that the short-circuiting current that flows through the inverting amplifier 30 of the crystal oscillation circuit of this embodiment is greatly reduced, making it possible to reduce the power consumption thereof.

The reasons for this are discussed below.

A timing chart of a prior-art crystal oscillation circuit is shown in Fig. 2 and a timing chart of the crystal oscillation circuit of this embodiment is shown in Fig. 3. In each of these figures, the elapsed time from the application of the power voltage V_{reg} from the power supplying circuit section 60 is plotted along the horizontal axis, with the feedback input $V_{G(t)}$ to the inverting amplifier 30 and the on/off state of the transistors 42 and 52 being plotted along the vertical axis.

As previously mentioned, the threshold voltages of the two transistors that configure the inverting amplifier of the prior-art crystal oscillation circuit are set in such a manner that the above Equation (1) is satisfied. The relationships between the threshold voltages of these transistors, the ground potential V_{DD}, and the power source potential V_{reg} in this case are shown graphically in Fig. 4. In other words, if the value of the feedback input $V_{G(t)}$ to the inverting amplifier is set to within the following range with respect to the potentials of the threshold voltages V_{TP} and V_{TN}:

$$V_{TP} > V_{G(t)} > V_{TN}$$

both transistors are turned on and a short-circuiting period is established thereby.

Therefore, while these transistors are being turned on and off alternately by the feedback signal $V_{G(t)}$, a time during which both of the transistors are driven to be on occurs periodically, as shown in Fig. 2, so that a short-circuiting current flows from the high potential (V_{DD}) to the low potential (V_{reg}) side, which is an impediment to any reduction in the power consumption.

In contrast thereto, the threshold voltages of the transistors 42 and 52 in this embodiment are set in such a manner that the above Equations (2) and (3) are satisfied. The relationships between the threshold voltages, the ground potential V_{DD}, and the power source potential V_{reg} in this case are shown in Fig. 5. That is to say, if the value of the feedback input $V_{G(t)}$ to the inverting amplifier 30 is set to be within the following range with respect to the potentials of the threshold voltages V_{TP} and V_{TN}:

$$V_{TN} > V_{G(t)} > V_{TP}$$

the two transistors 42 and 52 are turned firmly off so that there is no common-on time during which both of the transistors 42 and 52 are on, as there is in the prior art.

In other words, as shown in Fig. 3, while the transistors 42 and 52 are being driven on and off alternately by the feedback signal $V_{G(t)}$, there is no period of time during which both of the transistors 42 and 52 are on, so that the short-circuiting current that causes problems in the prior art is greatly reduced and thus the power consumption of the crystal oscillation circuit can be reduced.

In particular, this method of countering the short-circuiting current of the inverting amplifier 30 of this embodiment can be implemented without increasing the number of circuit components.

Furthermore, the absolute values of the threshold

voltages of the transistors 42 and 52 of this embodiment are each set to be less than the absolute value of the power voltage V_{reg}, as shown by Equations (3). This makes it possible to implement a reduced power consumption while maintaining a stable oscillation of the crystal oscillation circuit.

In other words, the absolute value of the amplitude of the feedback signal $V_{G(t)}$ of the inverting amplifier 30 in the crystal oscillation circuit does not exceed the absolute value of the power voltage V_{reg} of the inverting amplifier. This means that the transistors 42 and 52 can be driven to turn on and off alternately in a stable manner by setting the absolute values of the threshold voltages of the transistors 42 and 52 to satisfy Equations (3).

Experiments performed by the present inventors have verified that a satisfactory oscillation state can be maintained and the power consumption can be reduced when an oscillation circuit is driven by a power voltage V_{reg} of an absolute value of 0.9 volts, even when the sum of the absolute values of the threshold voltages of the transistors 42 and 52 varies within the following range:

$$1.4 \text{ volts} > |V_{TP}| + |V_{TN}| > 0.9 \text{ volts}$$

In addition, the off-leakage currents of the transistors 42 and 52 in this embodiment are reduced, for reasons that will be described below, making it possible to further reduce the power consumption of the entire circuit.

A characteristic graph of the relationship between the drain current I_D of an enhancement-mode transistor and the voltage V_{GS} between the gate and source thereof is shown in Fig. 6. It can be seen from this graph that the I_D-V_{GS} characteristic curve of an enhancement-mode transistor shifts towards the left and the off-leakage current thereof increases, as shown by the broken lines in the figure, as the threshold voltage is made lower (in this graph, the transistor turns off when V_{GS} is equal to or less than the threshold voltage V_{TH}, but at this region, the current I_D is yet to flow through the transistor as the off-leakage current, as shown by the broken lines in the figure).

Therefore, if the threshold voltages of the transistors 42 and 52 are set to be low, as in the prior-art oscillation circuit, the off-leakage current at and below the threshold voltage is larger, and the power consumption is incr ased by that amount.

In contrast thereto, since the threshold voltages of the transistors 42 and 52 in this embodiment are set to large values, as shown by Equation (2), the values of the off-leakage currents that flow through the transistors 42 and 52 are greatly reduced, and thus the power consumption of the entire circuit can be reduced.

Second Embodiment

The first embodiment was described above as being configured in such a manner that the threshold voltages of the transistors 42 and 52 satisfied Equation (2) to reduce the short-circuiting current, by way of example. This second embodiment of the invention makes it possible to reduce the short-circuiting current of the inverting amplifier 30 in a manner similar to that of the first embodiment, by applying direct current (DC) bias voltages to the gates of the transistors 42 and 52, even when those transistors 42 and 52 are configured to satisfy the condition of Equation (1), as in the prior art.

The crystal oscillation circuit of this embodiment is shown in Fig. 7 and a timing chart thereof is shown in Fig. 8.

This crystal oscillation circuit comprises a first bias circuit 70 and a second bias circuit 80 that each cause a shift in the DC potential of the feedback input $V_{G(t)}$ of the inverting amplifier 30 that is input to the gates of the transistors 42 and 52.

These bias circuits 70 and 80 each comprises a capacitor 72 or 82 for removing the DC component, and a resistor 74 or 84 for applying a DC bias voltage.

The capacitors 72 and 82 are used to remove the DC component from the gate signal $V_{G(t)}$ and apply the resultant signal to the gates of the corresponding transistors 42 and 52.

The resistor 74 is connected between the gate of the transistor 42 and the ground potential V_{DD}, to pull the DC potential of the feedback input $V_{G(t)}$ that is input to the gate of the transistor 42 up to the ground potential V_{DD}.

The resistor 84 is connected between the gate of the transistor 52 and the power voltage V_{reg}, to pull the DC potential of the feedback input $V_{G(t)}$ that is input to the gate of the transistor 52 down to the power source potential V_{reg}.

The above configuration ensures that the gate signal $V_{G(t)}$ that is input as feedback to the inverting amplifier 30 is applied to the gates of the transistors 42 and 52 in states in which the DC potential thereof has been converted to V_{DD} and the power source potential V_{reg} by the first and second bias circuits 70 and 80, as indicated by $V_{GP(t)}$ and $V_{GN(t)}$.

There is therefore is no period of time at which both of the transistors 42 and 52 are on while the transistors 42 and 52 are being driven to turn on and off alternately, and, as a result, the short-circuiting current flowing through the inverting amplifier 30 is greatly reduced, in a similar manner to that of the first embodiment, making it possible to reduce the power consumption.

In particular, this embodiment makes it possible to reduce the short-circuiting currents even when the absolute values of the threshold voltages of the enhancement-mode transistors 42 and 52 are made smaller. As a result, the power voltag applied to the inverting amplifier 30 is smaller, which also helps to

make it possible to reduce the power consumption.

Note that the bias voltages applied to the first and second bias circuits 70 and 80 could equally well be shifted in such a manner that the DC potentials of the feedback inputs to the gates of the transistors 42 and 52 are at potentials other than those of this embodiment, provided that the transistors 42 and 52 are not on simultaneously.

It should be noted that this invention is not limited to the above described embodiments, and it can be modified in various different ways within the range of the invention.

For example, the descriptions of the above embodiments were based on configurations in which each of the first and second circuits 40 and 50 had a single transistor, by way of example, but other configurations could be devised in which other circuit elements could be incorporated into the circuits if necessary, without causing any loss of function of the first and second circuits 40 and 50.

In addition, it is preferable that a semiconductor device is fabricated to comprise the crystal oscillation circuit of the above embodiments, or an electronic circuit that comprises such a crystal oscillation circuit, and this semiconductor device could be mounted in portable electronic equipment that has a restricted power source capacity, such as a portable telephone, a portable computer terminal, or any other type of portable equipment.

Furthermore, the descriptions of the above embodiments were based on the use of the crystal oscillation circuit in an electronic circuit for a timepiece, by way of example, but the present invention is not limited thereto. It has many other applications and is extremely effective when used in a wide range of portable electronic equipment that have restricted power source capacities, such as portable telephones, portable computer terminals, or any other type of portable equipment.

Variations

The description now turns to other oscillation circuits that make it possible to reduce the power consumption, most obviously when the oscillation circuit is activated and when it is operating stably, as well as electronic circuitry, a semiconductor device, electronic equipment, and a timepiece that use such oscillation circuits.

Another oscillation circuit in accordance with this invention comprises an inverting amplifier and a feedback circuit that has a crystal oscillator connected between the output and input sides of the inverting amplifier, for causing the phase of an output signal from the inverting amplifier to invert and feeding the thus inverted signal back to the inverting amplifier as an input. In this case, the inverting amplifier comprises a first circuit which is connected to the side of a first potential and which comprises a first semiconductor switching element that is driven to turn on and off by the feedback input, to excite the crystal oscillator, and a second circuit which is connected to the side of a second potential that differs from the first potential and which comprises a current-limiting element that limits the charge/discharge current that is generated by the oscillation of the crystal oscillator.

When a voltage is applied to the inverting amplifier of this crystal oscillation circuit, excitation of the crystal oscillator starts. During this time, the phase of the output from the inverting amplifier is inverted and fed back as an input by the feedback circuit. The operations of inverting, amplifying, and outputting this feedback input signal by the inverting amplifier are repeated.

The thus-repeated operations ensure that the oscillation of the crystal oscillator is increased gradually until the oscillation state of this oscillation circuit becomes stable.

In this embodiment of the invention, the inverting amplifier is configured of the first circuit, which is connected to the first potential side of the power source and which comprises the first semiconductor switching element, and the second circuit which has the current-limiting element and is connected to the second potential side of the power source.

The first semiconductor switching element is driven to turn on and off by the feedback input of the inverting amplifier, to drive the crystal oscillator. The current-limiting element limits the charge/discharge current that is generated by the oscillation of the crystal oscillator, to control the discharge of electrical energy stored in the crystal oscillator.

In other words, the prior-art crystal oscillation circuit has a circuit configuration such that the two transistors provided in the inverter are turned on and off alternately, and the crystal oscillator is discharged without any hindrance. This means the crystal oscillator must be recharged sufficiently in the next cycle, which increases the power consumption of the oscillation circuit.

In contrast thereto, this embodiment employs a configuration in which, when there is a discharge from the crystal oscillator in this embodiment, the current-limiting element of the second circuit ensures that the charging and discharging currents are limited to small values. This makes it possible to reduce the amount of power supplied during the charging part of the charge/discharge cycle of the crystal oscillator. As a result, the power consumption of the crystal oscillation circuit can be greatly reduced when it is oscillating stably.

In addition, this configuration of this embodiment is such that only the first semiconductor switching element configured of an inverting amplifier is driven to turn on and off when the crystal oscillation circuit is oscillating stably. This means that the inverting amplifier can be driven stably by applying a voltage V that takes into account the threshold voltage of this first semiconductor switching element to the inverting amplifier. Therefore, the voltage applied to the inverting amplifier can be

greatly reduced, and this reduction makes it possible to cut the power consumption even further, in an efficient manner.

In this embodiment, the second circuit could also use a resistor element as the current-limiting element.

The circuit configuration in that case is preferably such that one end of this resistor element is connected to the second potential side and the other end thereof is connected to the output side of the inverting amplifier.

This configuration makes it possible to simplify the structure of the second circuit.

The second circuit could also use the second semiconductor switching element as the current-limiting element.

The circuit configuration in that case may be such that one end of the second semiconductor switching element is connected to the second potential side and the other end thereof is connected to the output side of the inverting amplifier, to ensure off-control during stable oscillation.

This configuration makes it possible to simplify the circuit structure, even when a semiconductor switching element is used as the current-limiting element, and also makes it possible to set the applied voltage to a low level during stable oscillation.

The second semiconductor switching element may be connected to the second potential side, and the second circuit may be provided with a switching element control means. This switching element control means can drive the second semiconductor switching element by the feedback input at a timing differing from that of the first s miconductor switching element when the circuit is activated, to excite the crystal oscillator. After the oscillation has stabilized, the second semiconductor switching element is controlled by the switching element control means to be turned off and function as the current-limiting element.

This configuration makes it possible to excite the crystal oscillator when the circuit is activated by alternately turning the first and second switching elements on and off, in the same way as in the prior-art oscillation circuit, and achieve a stable oscillation state within a short time. After the oscillation has stabilized, the second semiconductor switching element is controlled to turn off, making it possible to effectively cut the power consumption of the entire circuit.

Note that when a depletion-mode transistor is used as the second semiconductor switching element, controlling the turning off of the second semiconductor switching element ensures that the potential difference between the gate and source thereof is small, thus limiting the current flowing therethrough.

The first semiconductor switching element can be configured by using an enhancement-mode field-effect transistor element, where the source thereof is connected to the first potential side, the feedback input is supplied to the gate thereof, and the drain is connected to the inverter output side.

This makes it possible to effectively limit the leakage current when the turning off of the first semiconductor switching element is being controlled, by using an enhancement-mode field-effect transistor element with a large threshold voltage as the first semiconductor switching element, thus achieving a more stable oscillation.

The second semiconductor switching element could be configured by using a depletion-mode field-effect transistor element, where the source thereof is connected to the second potential side, the feedback input is supplied to the gate thereof, and the drain is connected to the inverter output side.

This makes it possible to allow a current to pass to a certain extent, even when the field-effect transistor element is controlled to be off, by using a depletion-mode field-effect transistor element as the second semiconductor switching element. This enables the charge/discharge currents to flow from the crystal oscillator to a certain extent during the charge/discharge cycle of the crystal oscillator, making it possible to maintain a more stable oscillation state.

In other words, an enhancement-mode field-effect transistor element could be used as the second semiconductor switching element, but that configuration would ensure that the current discharging circuit from the crystal oscillator through the second semiconductor switching element would be completely cut off while the element is controlled to be off. In such a case, a certain amount of discharge will be caused by the discharging circuit of the crystal oscillator and by the various circuits connected in parallel with the crystal oscillator. If it is assumed that there is absolutely no discharge from the crystal oscillator, the oscillation will be basically maintained by the inertia of the crystal oscillator itself.

In contrast thereto, by using a depletion-mode field-effect transistor element as the second semiconductor switching element, this embodiment ensures that the second semiconductor switching element functions to permit discharging to a certain extent, while limiting the charge/discharge currents, in the same manner as a high-resistance resistor. This ensures that the oscillation of the crystal oscillation circuit can be made even more stable.

The first and second semiconductor switching elements could be configured by using field-effect transistor elements of differing conductivity types.

Furthermore, the oscillation circuit of this embodiment could further comprise a power circuit for supplying a power voltage at the first and second potentials. This power circuit could be configured to supply a first power voltage at activation that has a large potential difference between the first and second potentials, and a second power voltage after the oscillation has stabilized that has a potential difference which is smaller than that of the first power voltage but larger than the absolute value of the threshold voltage of the first semiconductor switching element.

In this manner, the oscillation of the circuit is raised to a stable state in a short time by a comparatively large first power voltage when the circuit is activated, then the oscillation circuit is driven by the second, lower power voltage. This makes it possible to solve two problems of the prior art, by establishing the oscillation circuit rapidly and cutting the power consumption.

A crystal oscillator with a large Q value may be used as this crystal oscillator.

This makes it possible to maintain the stable oscillation state at an even lower power consumption after the oscillation has stabilized, by using a crystal oscillator that has a large value of Q, which represents the ease with which the oscillator vibrates mechanically.

It is also possible to reduce the power consumption of a timepiece or an item of portable electronic equipment, such as a portable telephone or computer terminal, by using an oscillation circuit of the above configuration in the fabrication of an electronic circuit, a semiconductor device, electronic equipment, or a timepiece, and thus reduce the consumption thereof of power from an internal battery or secondary battery.

Specific configurations of such portable electronic equipment are described below with reference to the accompanying drawings.

An example of such a crystal oscillation circuit is shown in Fig. 9. The crystal oscillation circuit of this embodiment is one that is used in a quartz wristwatch. Note that components that correspond to those in Fig. 1 are given the same reference numbers in this figure and further description thereof is omitted.

In the same way as in previous embodiments, the crystal oscillation circuit of this embodiment comprises the inverting amplifier 30, the crystal oscillator 10, and a feedback circuit.

The inverting amplifier 30 comprises the first circuit 40 and the second circuit 50.

The first circuit 40 comprises the p-type field-effect transistor 42 that functions as a first semiconductor switching element. The source of this transistor 42 is connected to ground, the drain thereof is connected to an output terminal 79, and the feedback signal $V_{G(t)}$ is applied to the gate thereof.

The second circuit 50 comprises a resistor 94 that functions as a current-limiting element. One end of this resistor 94 is connected to the output terminal 79 side (in this case, it is connected to the drain of the transistor 42) and the other end thereof is connected to the power source terminal side of the power supplying circuit section 60.

A timing chart of the crystal oscillation circuit of this embodiment is shown in Fig. 10, where the elapsed time from the application of the power voltage V_{reg} from the power supplying circuit section 60 is plotted along the horizontal axis and the feedback input $V_{G(t)}$ and oscillation output $V_{D(t)}$ of the inverting amplifier 30 are both plotted along the vertical axis. Note that, in this case, V_{DD} represents the ground potential and V_{TP} the threshold voltage of the field-effect transistor 42. Since a p-type, enhancement-mode field-effect transistor is used in this case, the threshold voltage V_{TP} thereof is a negative value.

First of all, if the power voltage V_{reg} from the power supplying circuit section 60 is applied to the inverting amplifier 30, the crystal oscillation circuit starts to oscillate as shown in Fig. 10. In this graph, T_1 represents the oscillation growth period from when the voltage is applied until a stable oscillation state is reached, and T_2 represents a stable oscillation period during which the oscillation output is stable.

If a gate voltage $V_{G(t)}$ that is equal to or less than the threshold voltage is applied to the gate of the transistor 42, as shown by 100-1, the transistor 42 is turned on, a current flows in the direction of an arrow 300 in Fig. 9, and the drain signal $V_{D(t)}$ which is the inversion of the gate signal $V_{G(t)}$ is output from the inverting amplifier 30. In this way, the drain signal $V_{D(t)}$ is output from the crystal oscillation circuit, as shown by 200-1.

The crystal oscillator 10 starts to be charged and excited by the current indicated by the arrow 300.

During this time, the phase of the output $V_{D(t)}$ of the inverting amplifier 30 is inverted through 180 degrees by the feedback circuit formed of the resistor 14 and other components, is output as the gate signal $V_{G(t)}$, and is fed back as an input to the gate of the transistor 42. Therefore, the gate signal $V_{G(t)}$ that is fed back exceeds the threshold voltage V_{TP} in the next cycle 100-2. This controls the transistor 42 to turn off.

In this time, the charged energy of the crystal oscillator 10 is discharged through the resistor 94, as shown by an arrow 310 in Fig. 9. Therefore, the output voltage $V_{D(t)}$ of the oscillation circuit gradually decreases, as shown by 200-2 in Fig. 10.

The oscillation output $V_{D(t)}$ gradually increases and becomes stable while the charge/discharge cycle is repeated in this manner, and the oscillation state of the circuit transits from the oscillation growth period T_1 to the stable oscillation period T_2.

In Fig. 10, 100-1, 100-3, 100-5, 100-7... denote periods during which a voltage that is less than or equal to the threshold voltage is applied to the gate of the transistor 42 and the transistor 42 is on, and 100-2, 100-4, 100-6, 100-8... denote periods during which the transistor 42 is conversely controlled to be off.

Similarly, 200-1, 200-3, 200-5, 200-7... denote the oscillation output $V_{D(t)}$ when the transistor 42 is on and 200-2, 200-4, 200-6, 200-8... denote the oscillation output $V_{D(t)}$ when the transistor 42 is off. As shown in this figure, the oscillation output $V_{D(t)}$ is centered on a voltage ($V_{reg}/2$) that is half the voltage V_{reg}, and is alternately inverted for output.

In the crystal oscillation circuit of this embodiment, the discharging current of the excitation energy that is charged into the crystal oscillator 10 is controlled by the resistor 94 during the discharging cycles 200-2, 200-4, 200-6, 200-8... of the crystal oscillator 10 shown in Fig.

10, so that this discharging current is at the minimum necessary.

This ensures that the energy for charging the crystal oscillator 10 in the next charging cycle is reduced, making it possible to greatly cut the power consumption of the crystal oscillation circuit as a result.

A particular feature of the crystal oscillation circuit of this embodiment is the way in which a large resistor is used as the resistor 94, greatly limiting the discharging current. In addition, an enhancement-mode transistor is used as the transistor 42, which completely cuts off the current 300 during off-control.

This makes it possible to reduce the discharging energy in the discharging cycles 200-6, 200-8, 200-10... during the stable oscillation period T_2, as well as making it possible to maintain a stable oscillation state, as shown in Fig. 10.

In other words, the two problems of oscillating the entire circuit stably and cutting the power consumption can be solved by supplying the minimum energy necessary for maintaining the oscillation at a timing matched to the oscillation, when the circuit is oscillating stably, that is to say, at the timing of 100-7, 100-9....

Note that it is preferable to use a crystal oscillator with a large Q value as this crystal oscillator 10. This ensures that energy losses due to mechanical vibrations are low when the circuit is oscillating stably, so that a sufficiently large electrical output can be fed back as an input by the crystal oscillator 10 to the gate of the inverting amplifier 30. Therefore the crystal oscillation circuit can be driven in oscillation with an even lower power consumption and also stably.

In particular, the feedback efficiency of the output from the inverting amplifier 30 is increased by employing the above configuration, so that a smaller output from the inverting amplifier 30 will suffice. As a result, the power voltage V_{reg} of the inverting amplifier 30 can be made smaller, and thus the power consumption of the entire circuit can be reduced.

In other words, the inverting amplifier 30 of this embodiment uses only the field-effect transistor 42. If seen from the viewpoint of stable operation of the inverting amplifier 30, this means that the absolute value of the power voltage V_{reg} supplied from the power supplying circuit section 60 can be set to a value that exceeds the absolute value of the threshold voltage of that one transistor 42. Therefore the power voltage V_{reg} can be made greatly smaller than the value required for turning the two field-effect transistors on and off, as in the prior-art crystal oscillation circuit, and thus a crystal oscillation circuit with an even lower power consumption can be implemented.

If necessary, the crystal oscillation circuit could be configured by using the inverting amplifier 30 shown in Fig. 15 instead of the inverting amplifier 30 shown in Fig. 9.

In other words, the inverting amplifier 30 of Fig. 9 was described by way of example as having the first potential to which the first circuit 40 is connected as a ground potential side and the second potential to which the second circuit 50 is connected as the negative power potential V_{reg} side, but conversely the first potential to which the first circuit 40 is connected could be the negative power potential V_{reg} and the second potential to which the second circuit 50 is connected could be at the ground potential V_{DD}. In such a case, the circuit uses the resistor 94 to ensure that the charging current of the crystal oscillator 10 is limited, but a similar effect as that of Fig. 9 can also be employed therefor.

Another embodiment of the crystal oscillation circuit is shown in Fig. 12. Note that components that correspond to those in Fig. 9 are given the same reference numbers in this figure and further description thereof is omitted..

This embodiment is characterized in that the current-limiting element 94 that configures the second circuit 50 of Fig. 9 is replaced by a field-effect transistor 54.

In this embodiment, a field-effect transistor which has n-type conductivity and is also a depletion-mode transistor is used as this field-effect transistor 54. The use of a depletion-mode field-effect transistor makes it possible for a current to flow to a certain extent between the drain and the source thereof, even when the transistor 54 is controlled to be off, and, as a result, this transistor 54 can be made to function as a current-limiting element that limits the current flowing therethrough.

The source of the transistor 54 is connected to the power voltage V_{reg} side of the power supplying circuit section 60 and the drain thereof is connected to the output terminal 79 of the oscillation circuit (in this case, it is actually connected to the drain of the other transistor 42). The fed-back gate signal $V_{G(t)}$ and a control signal 400 supplied from a control circuit section 90 are both input to the gate of the transistor 54 through an AND gate 92.

A timing chart of the crystal oscillation circuit of this embodiment is shown in Fig. 13. In this figure, $V_{GN(t)}$ represents a gate voltage applied to the gate of the transistor 54 from the AND gate 92.

In this embodiment, the control circuit section 90 detects whether or not the crystal oscillation circuit has reached a stable oscillation state after the power voltage V_{reg} has been applied to the crystal oscillation circuit.

The control circuit section 90 outputs a high-level control signal 400 to the AND gate 92 from the time that the power voltage is applied until the oscillation stable state is achieved, then the control signal 400 switches from high to low after the oscillation has stabilized.

This ensures that the gate signal $V_{G(t)}$ that is fed back and input to the gate of the transistor 54 is applied thereto without modification during the time that the control signal 400 is high, the two transistors 42 and 54 configuring the inverting amplifier 30 are alternately turned on and off by this gate signal $V_{G(t)}$, and thus the oscillation circuit can rise rapidly to a stable oscillation

state.

When the oscillation has stabilized, the level of the control signal 400 is switched to low so that the transistor 54 is forcibly controlled to stay off and the remaining transistor 42 alone is turned on and off, in the same way as in the embodiment of Fig. 9. During this time, since a depletion-mode transistor is used for the transistor 54 that is turned off, as described previously, the value of the discharging current in the discharging cycles of the crystal oscillator 10 can be greatly limited, making it possible to cut greatly the power consumption of the entire circuit.

This depletion-mode transistor 54 is also called a normally-on transistor because a drain current can still flow even when the voltage between the source and gate thereof is zero. For that reason, the value of the power voltage V_{reg} necessary for driving the inverting amplifier 30 stably can be set to that for the enhancement-mode field-effect transistor 42 alone, so that the value of the power voltage V_{reg} can be greatly reduced in comparison to the configuration in which both of the transistors 42 and 54 are enhancement-mode transistors, and this aspect can also help cut the power consumption.

In this manner, the crystal oscillation circuit of this embodiment can achieve stable oscillation within a short time, and can also make it possible to dramatically cut the power consumption when it is oscillating stably.

In this embodiment, the transistor 54 that functions as a current-limiting element is used actively only when the circuit is activated, and it becomes unnecessary for the oscillation operation once the oscillation is stable. This means that the capabilities of the transistor 54 can be made less that those of the other transistor 42, which is extremely effective from the circuit configuration viewpoint.

The circuit of this embodiment is configured by using transistors of differing conductivity types as the field-effect transistors 42 and 54 of the first and second circuits 40 and 50, but the circuit could equally well be configured so that transistors of the same conductive type (for example, p-type) are used for the field-effect transistors 42 and 54 of the first and second circuits 40 and 50.

Specific examples of circuit configurations in which the transistors 42 and 54 are p-type transistors are shown in Figs. 16 and 17. The inverting amplifier 30 shown in Fig. 16 is configured in such a manner that the transistor 42 is an enhancement-mode field-effect transistor, the transistor 54 is a depletion-mode field-effect transistor, and the gate of the depletion-mode field-effect transistor 54 that functions as a current-limiting element is connected to the ground V_{DD} side.

This configuration ensures that the field-effect transistor 54 of Fig. 16 functions in a similar manner to the field-effect transistor 54 of Fig. 12, making it possible to effectively limit the discharging current from the crystal oscillator 10.

The inverting amplifier 30 shown in Fig. 17 uses p-type enhancement-mode field-effect transistors for both of the transistors 42 and 54. The gate of the transistor 54 that functions as a current-limiting element is connected to the power source V_{reg} side. This circuit configuration ensures that the transistor 54 is always on but, if a high-impedance element is used for this always-on transistor 54, the transistor 54 can function as a current-limiting element to limit the discharging current from the crystal oscillator 10.

The embodiments of the crystal oscillation circuit shown in Figs. 9 and 12 were described as using a power voltage V_{reg} that is constant, by way of example, but a configuration that switches between a large value of V_{reg} during the oscillation growth period T_1 and a small value of V_{reg} during the stable oscillation period T_2 could also be used therefor. This makes it possible to achieve stable oscillation quickly, while enabling a cut in power consumption after the oscillation has stabilized.

In other words, the power supplying circuit section 60 in each of the crystal oscillation circuits of the embodiments shown in Figs. 9 and 12 is configured to switch between outputting a first power voltage V_{reg1} for activation and a second power voltage V_{reg2} for stable drive, as shown in Figs. 11 and 14. In such a case, the absolute value of the first power voltage V_{reg1} is set to be greater than the absolute value of the second power voltage V_{reg2}, so that the inverting amplifier 30 can be driven by a large power supply when the circuit is activated.

The control circuit section 90 outputs the control signal 400 to the power supplying circuit section 60 to control the power supplying circuit section 60 in such a manner that it outputs the first power voltage V_{reg1} when the circuit is activated and the second power voltage V_{reg2} when the oscillation has stabilized.

This makes it possible to greatly shorten the oscillation growth period T_1, in comparison with oscillation circuits that are driven continuously at the same power voltage, thus enabling rapid establishment of the oscillation circuit.

Note that various other embodiments of the present invention can be envisioned, in addition to the embodiments of Figs. 9 and 12.

For example, the second embodiment shown in Fig. 12 was described as using a depletion-mode transistor as the transistor 54, by way of example, but this embodiment is not limited thereto and it can equally well use any other type of transistor, such as an enhancement-mode transistor. In such a case, the discharging current denoted by 310 from the crystal oscillator 10 is completely cut while the transistor is controlled to be off, and this portion acts as a brake on the oscillation. However, a certain amount of leakage is possible from the crystal oscillator 10 itself and from the discharging circuit through the resistor 14, and moreover the crystal oscillator 10 will continue to oscillate naturally due to inertia, so that the oscillation of the crystal oscillator 10 can be

maintained thereby. In other words, the efficiency will drop to a certain extent in comparison to a the case in which the transistor 54 is a depletion-mode transistor, but the power consumption is still less than it is in the prior art and in addition a stable oscillation state can be maintained.

The first and second circuits 40 and 50 that form the inverting amplifier 30 were described above as using the transistor 42 and a first current-limiting element, respectively, by way of example, but other circuit elements can also be combined therein to configure these circuits if necessary, without any loss of function of the first and second circuits 40 and 50.

The descriptions of the above embodiments also took the use of the crystal oscillation circuit of this invention in an electronic circuit for a timepiece, by way of example, but the present invention is not limited thereto and is extremely effective when used a wide range of portable electronic equipment that have restricted power source capacities, such as portable telephones, portable computer terminals, or any other type of portable equipment.

Claims

1. An oscillation circuit comprising:

an inverting amplifier including a first semiconductor switching element and a second semiconductor switching element;

wherein said first and second semiconductor switching elements are prevented from being on simultaneously to limit a short-circuiting current flowing through said inverting amplifier when said first and second semiconductor switching element is driven.

2. The oscillation circuit as defined in claim 1,

wherein the sum of the absolute value of the threshold voltage of said first semiconductor switching element and the absolute value of the threshold voltage of said second semiconductor switching element is set to be greater than or equal to the absolute value of the power voltage of said inverting amplifier, to limit a short-circuiting current flowing through said inverting amplifier.

3. The oscillation circuit as defined in claim 1,

further comprising a feedback circuit having a crystal oscillator connected between the output and input sides of said inverting amplifier, for causing the phase of an output signal from said inverting amplifier to invert and feeding the thus inverted signal back to said inverting amplifier as an input;

wherein said inverting amplifier comprises a first circuit including said first semiconductor switching element, and a second circuit including said second semiconductor switching element;

wherein said first semiconductor switching element is connected to the side of a first potential and is driven to be turned on and off by said feedback input, to excite said crystal oscillator;

wherein said second semiconductor switching element is connected to the side of a second potential that differs from said first potential and is driven to be turned on and off by said feedback input at a timing that differs from that of said first semiconductor switching element, to excite said crystal oscillator; and

wherein the sum of the absolute value of the threshold voltage of said first semiconductor switching element and the absolute value of the threshold voltage of said second semiconductor switching element is set to be greater than or equal to the absolute value of the power voltage of said inverting amplifier, to limit a short-circuiting current flowing through said inverting amplifier.

4. The oscillation circuit as defined in claim 1,

further comprising a bias circuit for applying a first direct current bias voltage and a second direct current bias voltage to gates of said first semiconductor switching element and said second semiconductor switching element, respectively;

wherein said first and second direct current bias voltages shift the values of the direct current potentials of feedback inputs that are input from said inverting amplifier to said gates of said first and second semiconductor switching elements, to prevent said first and second semiconductor switching elements from being on simultaneously.

5. The oscillation circuit as defined in claim 1,

further comprising:

a feedback circuit having a crystal oscillator connected between the output and input sides of said inverting amplifier, for causing the phase of an output signal from said inverting amplifier to invert and feeding the thus inverted signal back to said inverting amplifier as an input; and

a bias circuit for applying a direct current bias voltage to said inverting amplifier;

wherein said inverting amplifier comprises:

a first circuit connected to the side of a first potential and comprising said first semiconductor switching element; and

a second circuit connected to the side of a second potential that differs from said first potential and comprising said second semiconductor switching element;

wherein said first semiconductor switching element is connected to the side of said first potential and is driven to be turned on and off by said feedback input that is input to a gate, to excite said crystal oscillator;

wherein said second semiconductor switching element is connected to the side of said second potential and is driven to be turned on and off by said feedback input that is input to a gate at a timing that differs from that of said first semiconductor switching element, to excite said crystal oscillator;

wherein said bias circuit comprises:

a first bias circuit for applying a first direct current bias voltage to the gate of said first semiconductor switching element; and

a second bias circuit for applying a second direct current bias voltage to the gate of said second semiconductor switching element; and

wherein said first and second direct current bias voltages shift the values of the direct current potentials of feedback inputs that are input from said inverting amplifier to said gates of said first and second semiconductor switching elements, to prevent said first and second semiconductor switching elements from being on simultaneously.

6. The oscillation circuit as defined in claim 5,

wherein said first direct current bias voltage is set to said first potential and said second direct current bias voltage is set to said second potential.

7. The oscillation circuit as defined in any one of claims 1 to 6,

wherein said first and second semiconductor switching elements are configured by using field-effect transistor elements of differing conductivity types.

8. An electronic circuit comprising the oscillation circuit as defined in any one of claims 1 to 7.

9. A semiconductor device comprising one of the oscillation circuit as defined in any one of claims 1 to 7, and the electronic circuit of claim 8.

10. Electronic equipment comprising one of the oscillation circuit as defined in any one of claims 1 to 7, and the electronic circuit of claim 8.

11. A timepiece comprising one of the oscillation circuit as defined in any one of claims 1 to 7, and the electronic circuit of claim 8.

FIG. 1

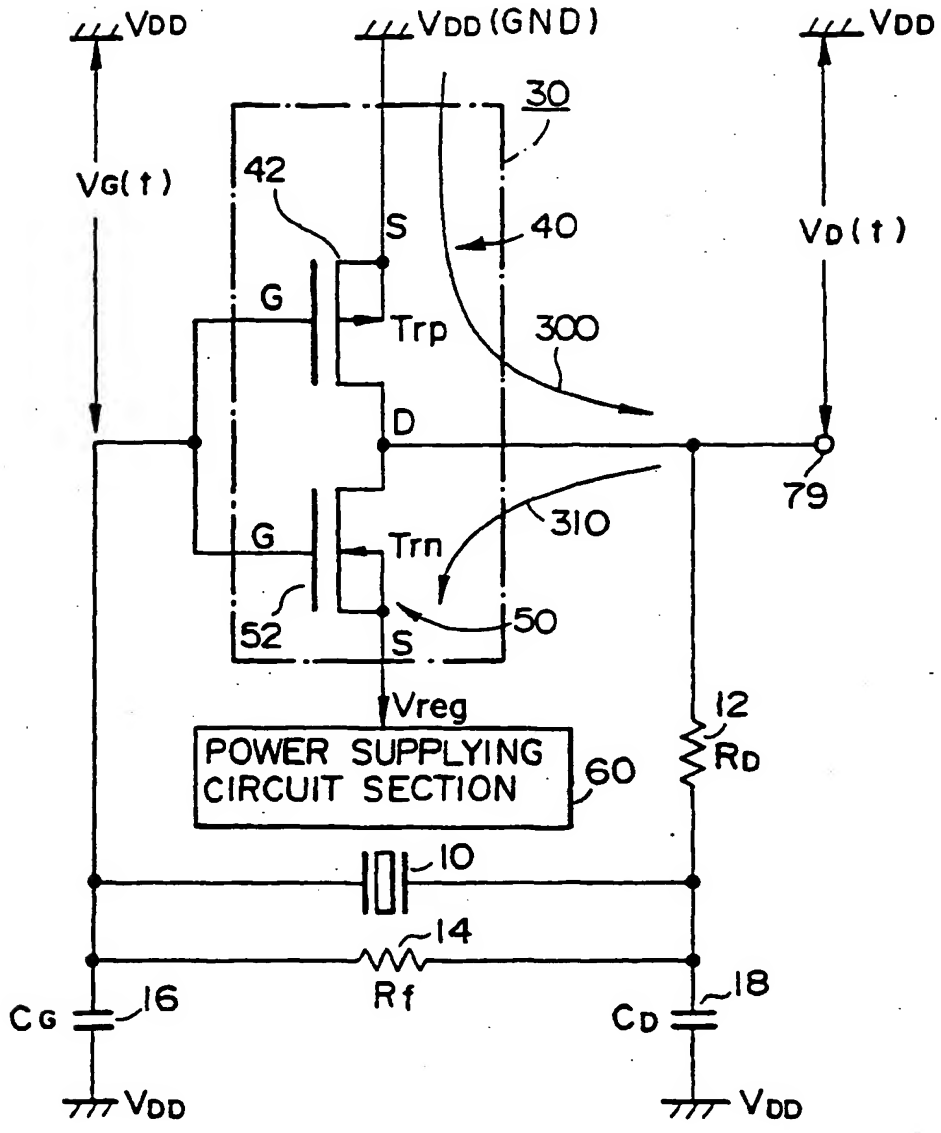

VDD
VDD (GND)
VDD
30
VG(t)
42
S
40
VD(t)
G
Trp
300
D
79
G
Trn
310
52
S
50
Vreg
12
POWER SUPPLYING CIRCUIT SECTION
60
RD
10
14
Rf
CG
16
CD
18
VDD
VDD

FIG. 2

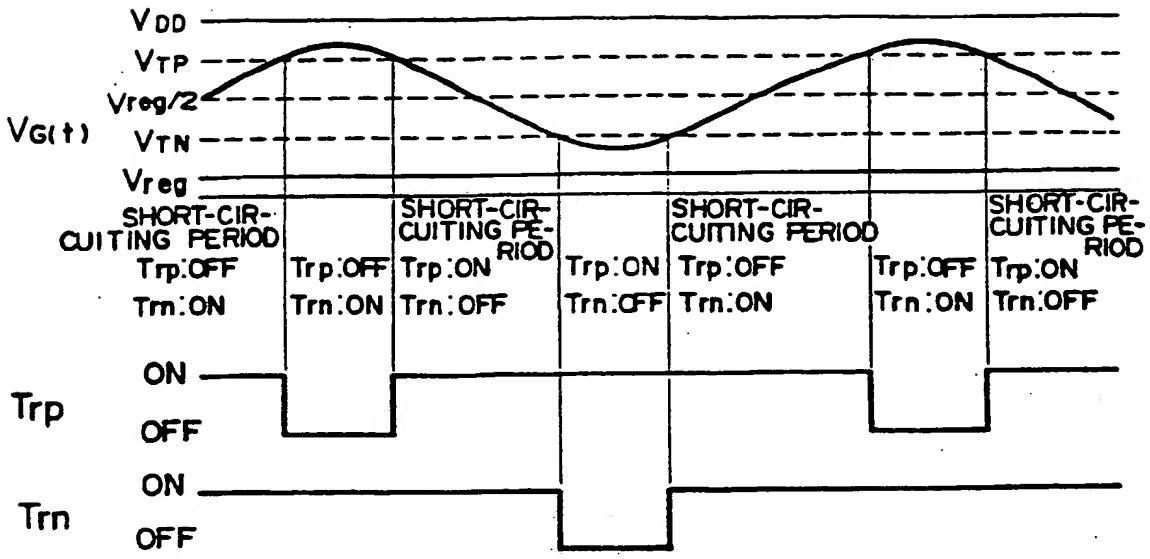


FIG. 3

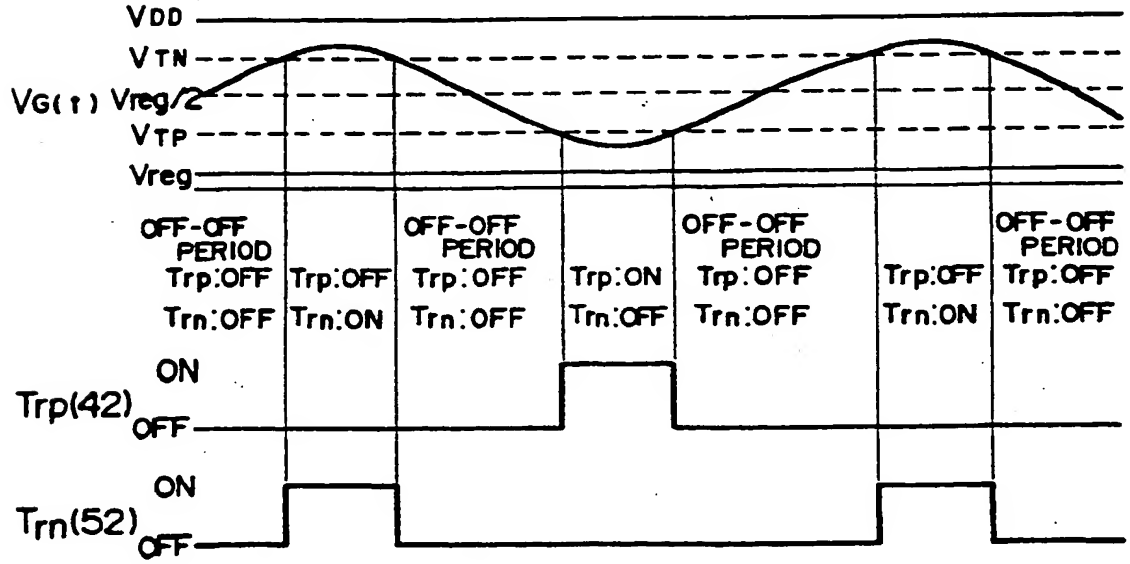


FIG. 4

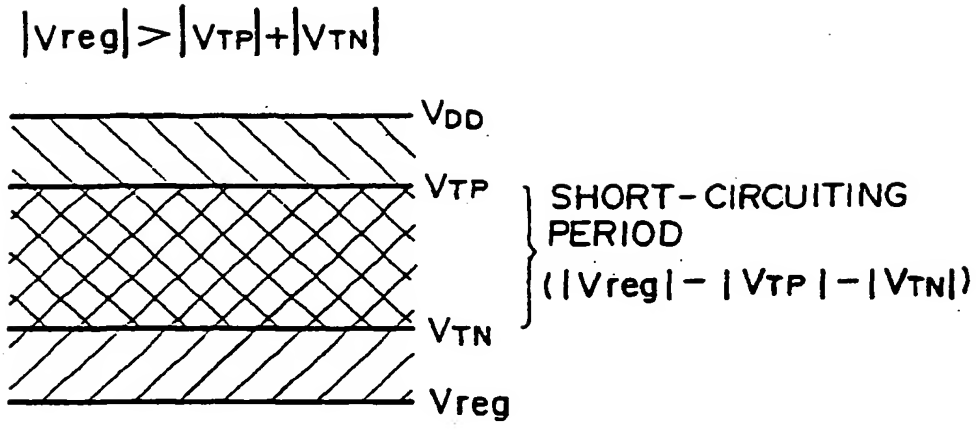


FIG. 5

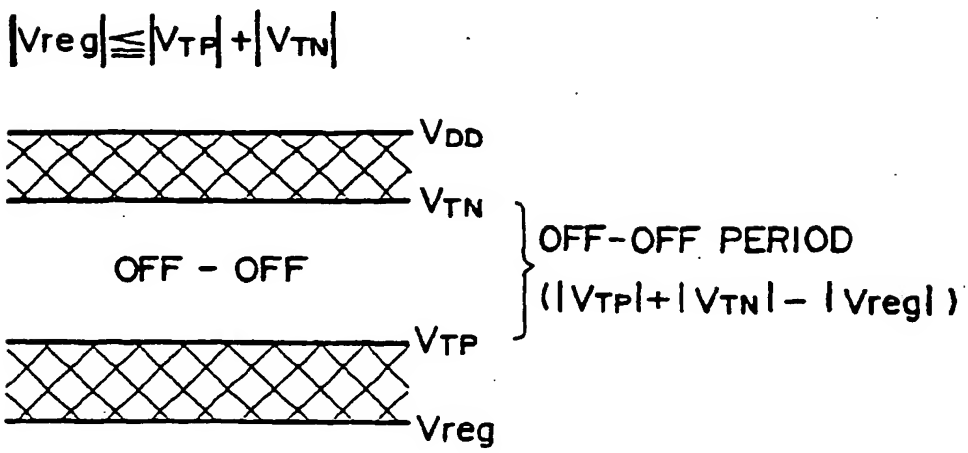


FIG. 6

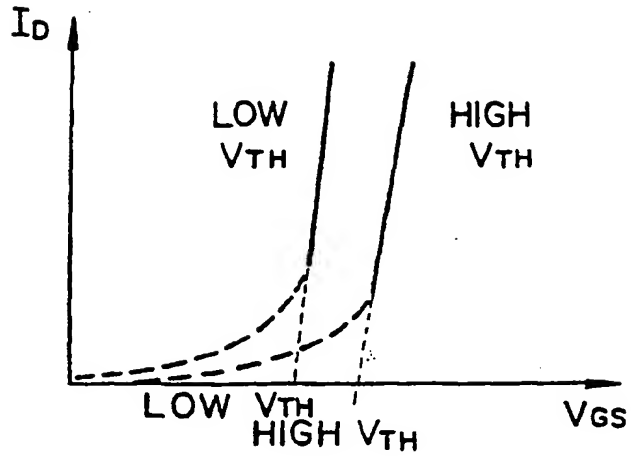


FIG. 7

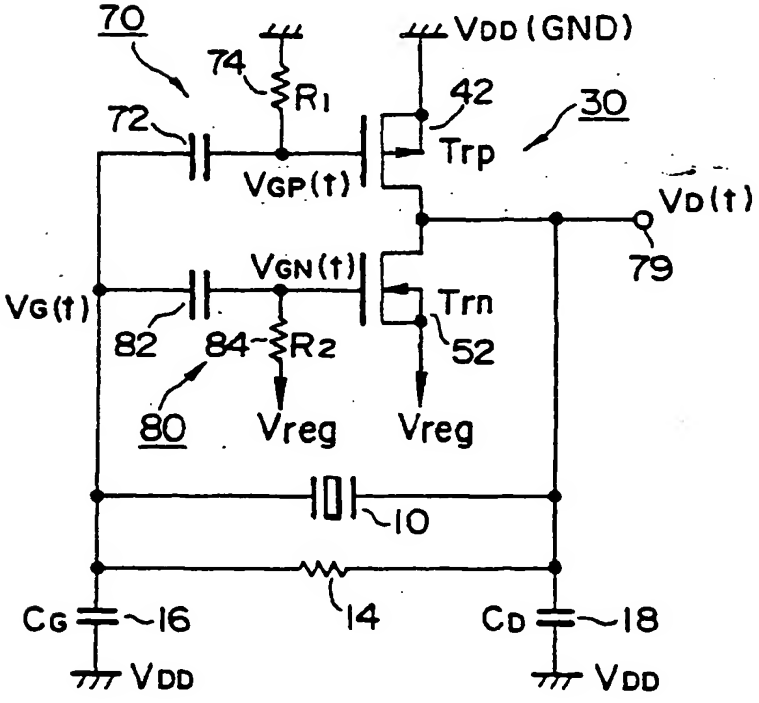
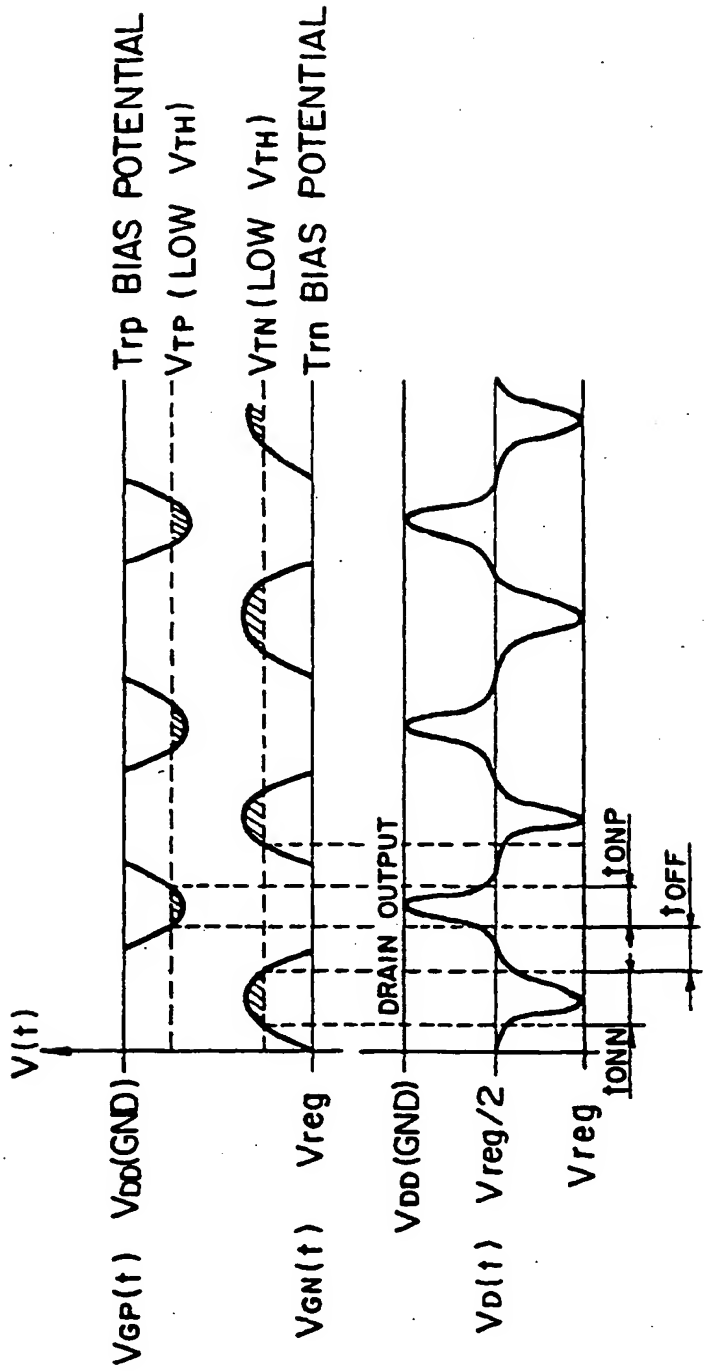


FIG.8



t_{ONN} : n-CHANNEL TRANSISTOR ON

t_{ONP} : p-CHANNEL TRANSISTOR ON

t_{OFF} : BOTH OF n-CHANNEL AND p-CHANNEL TRANSISTORS OFF

FIG. 9

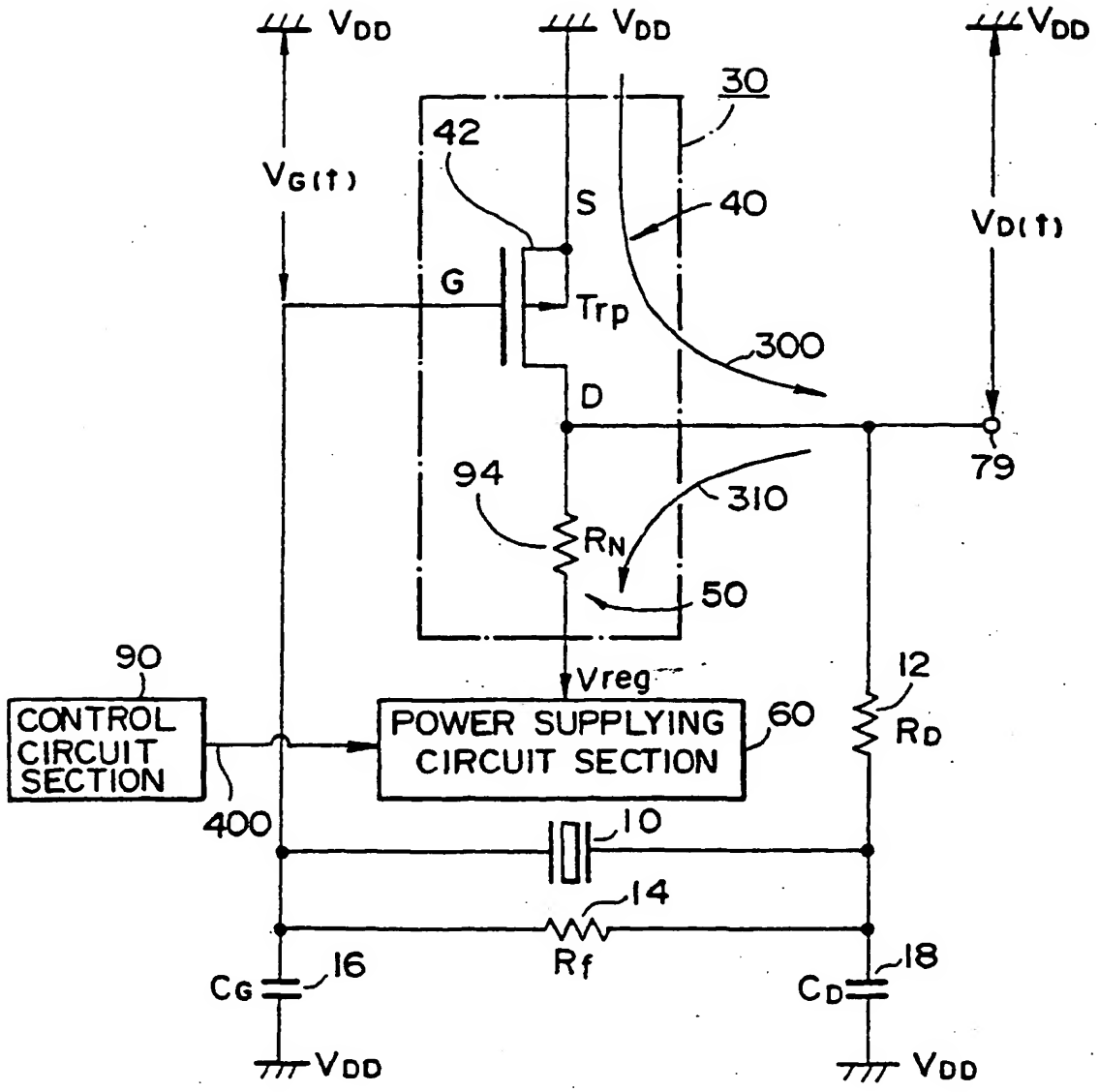


FIG. 10

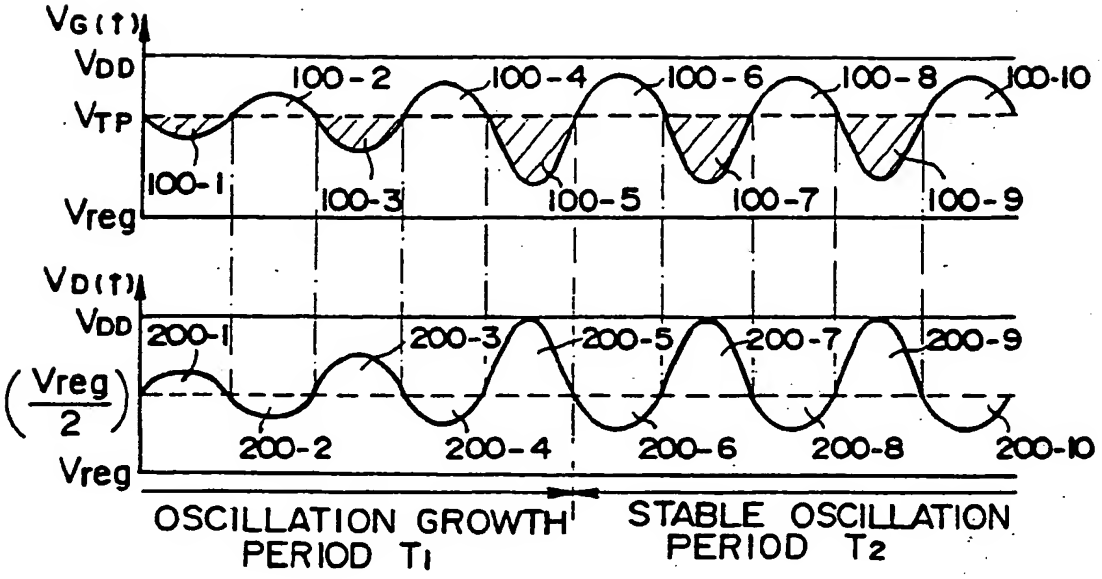


FIG. 11

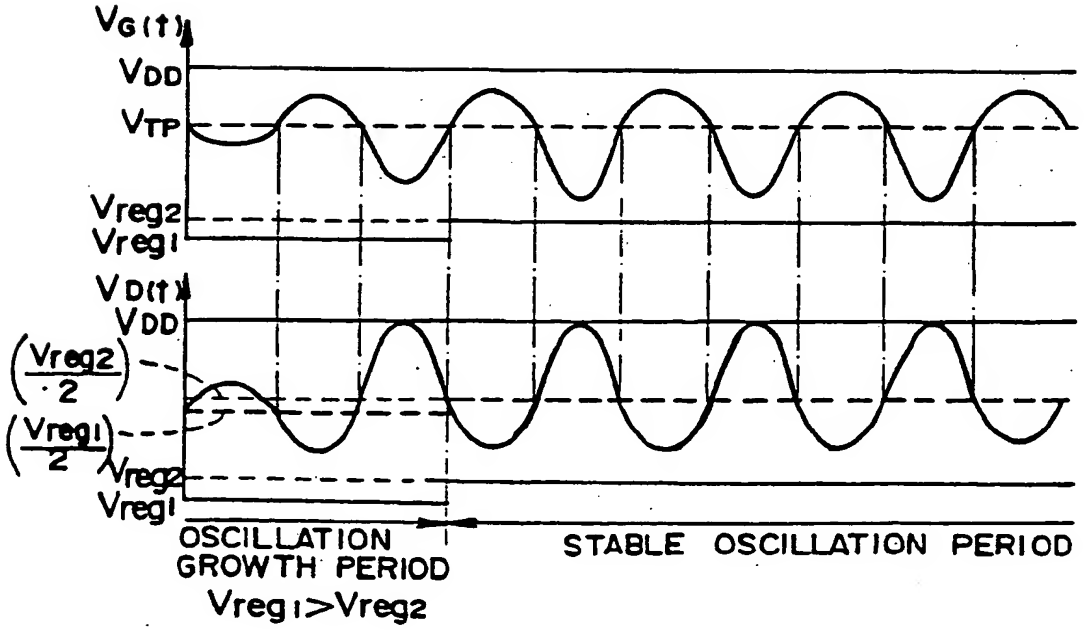


FIG. 12

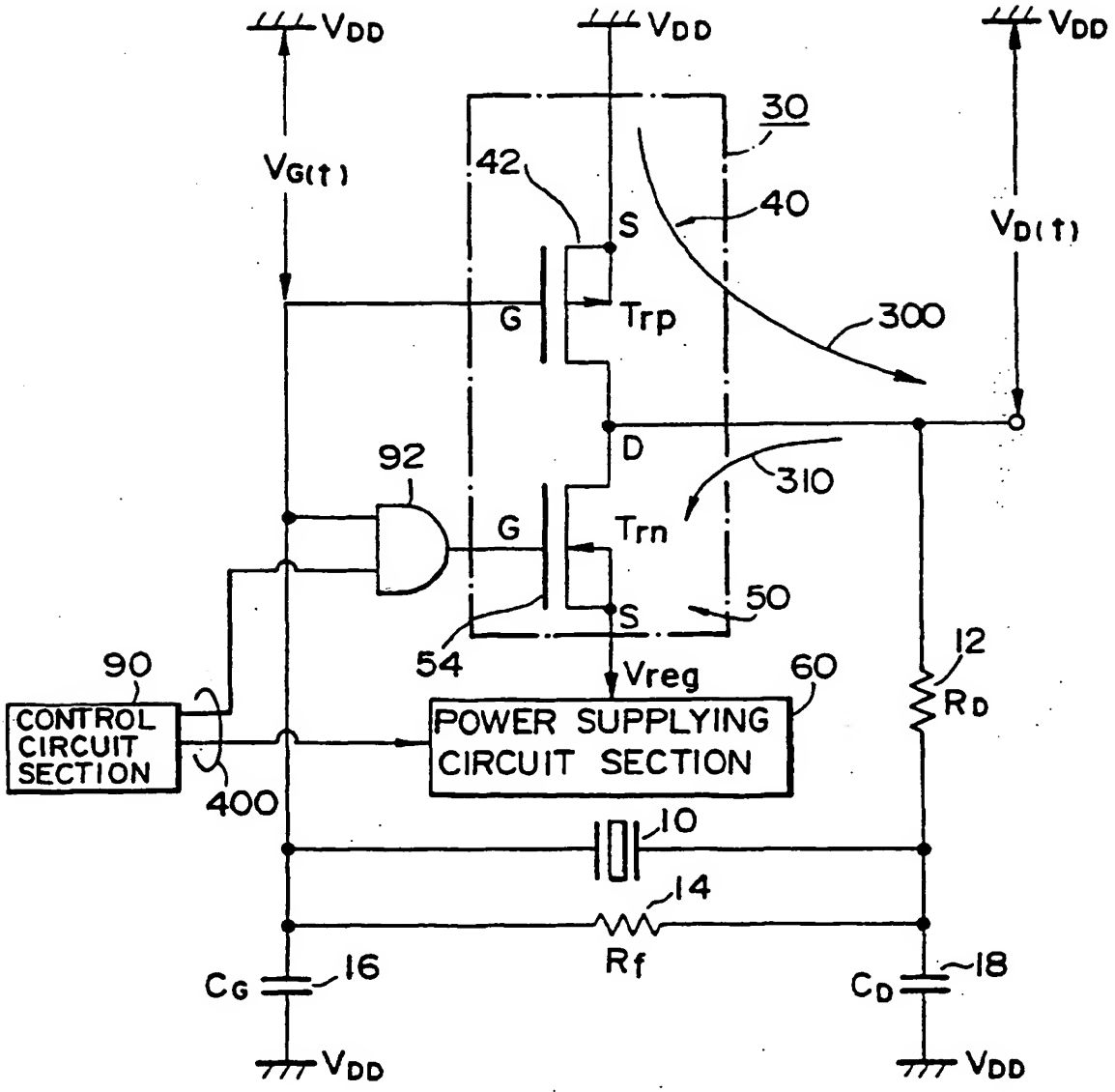


FIG. 13

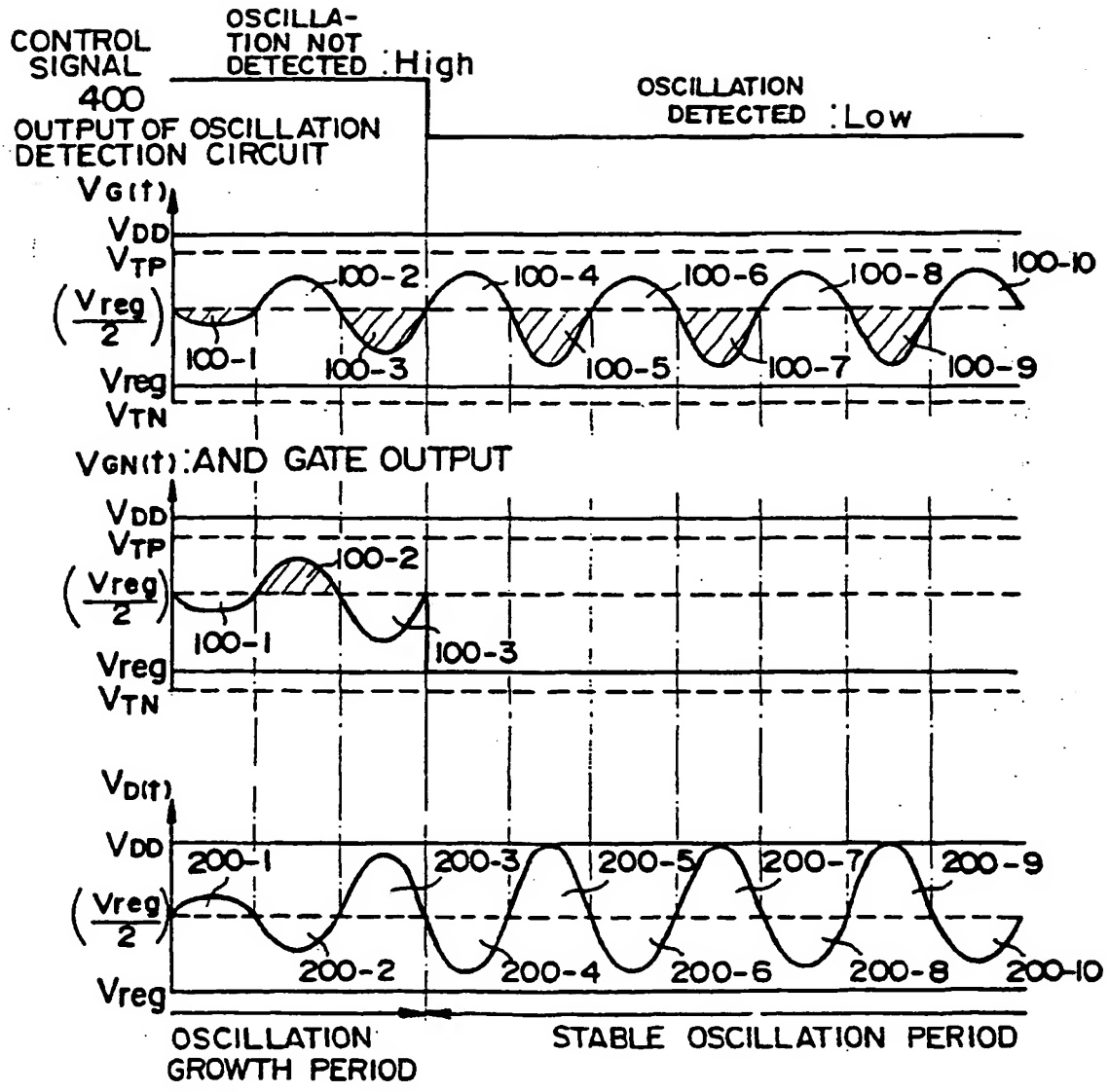


FIG. 14

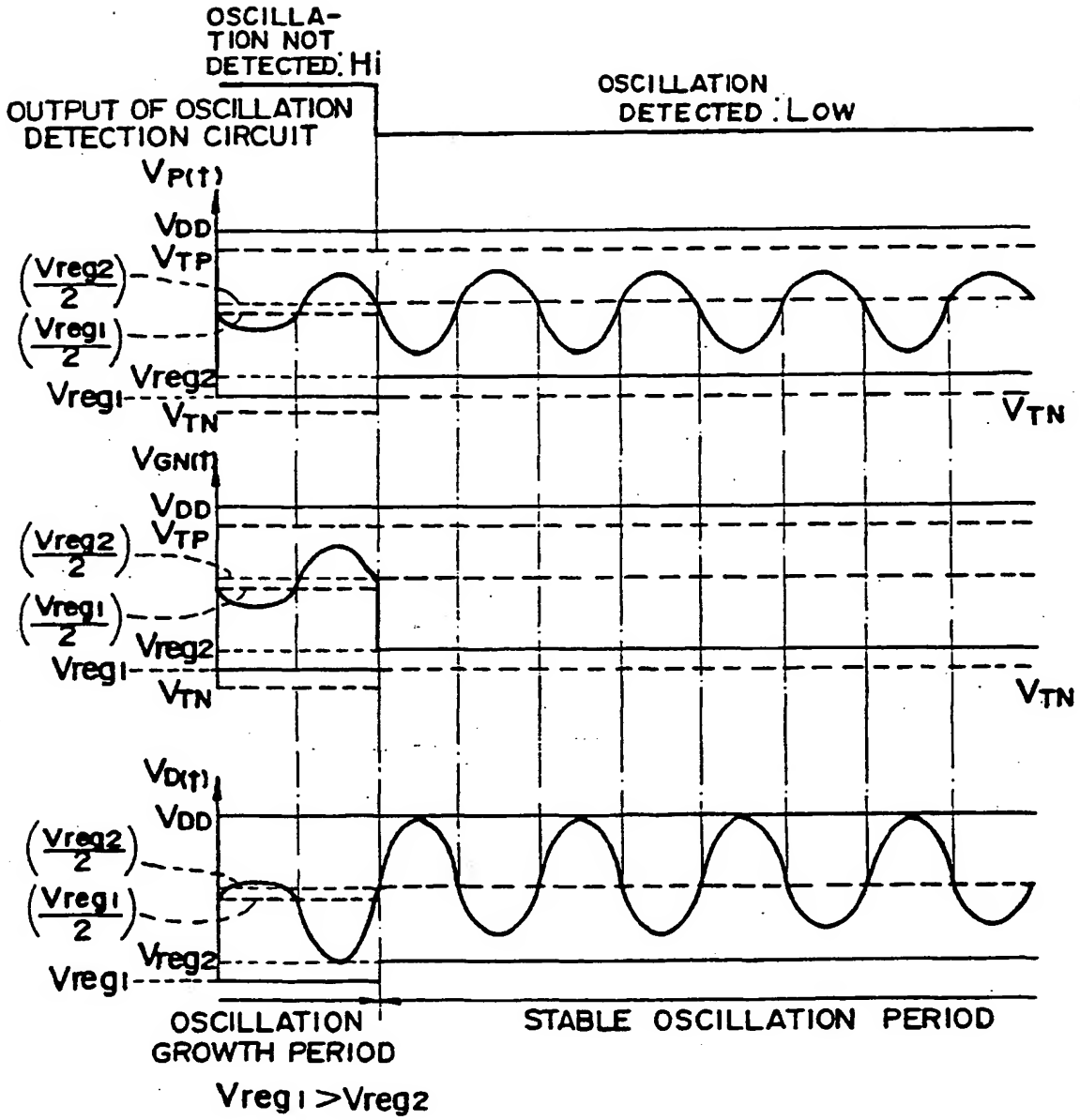


FIG. 15

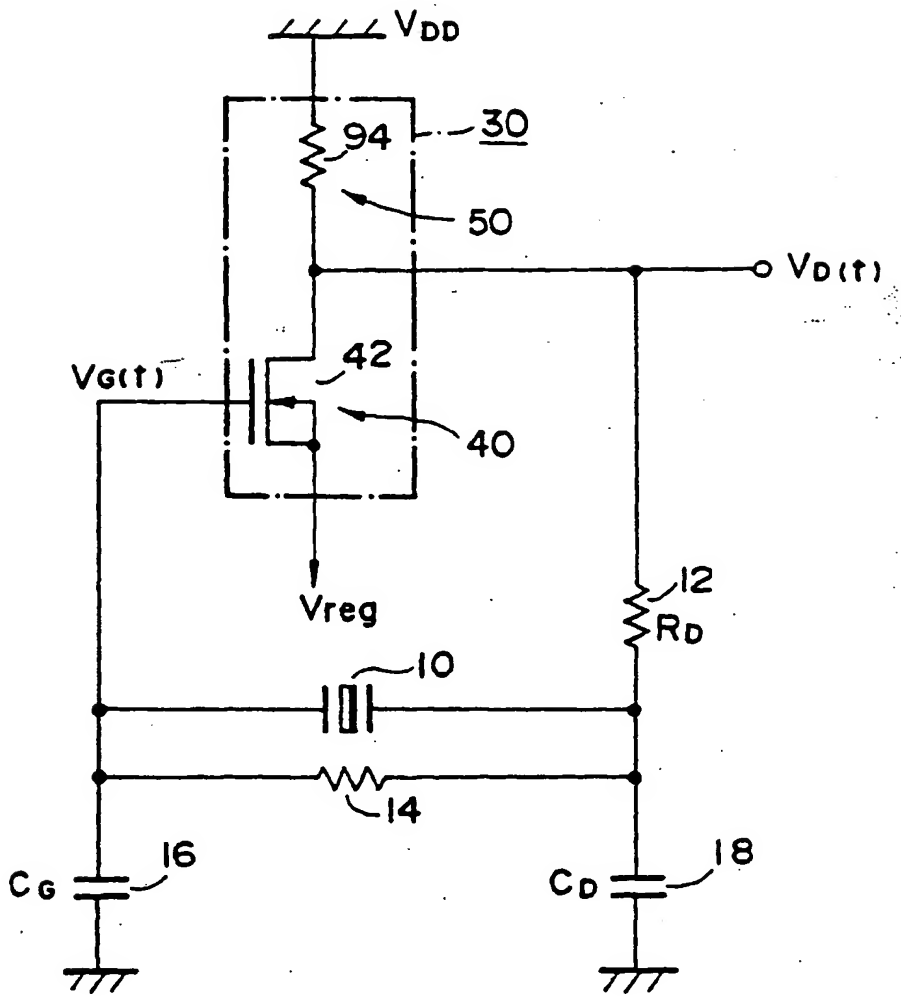


FIG. 16

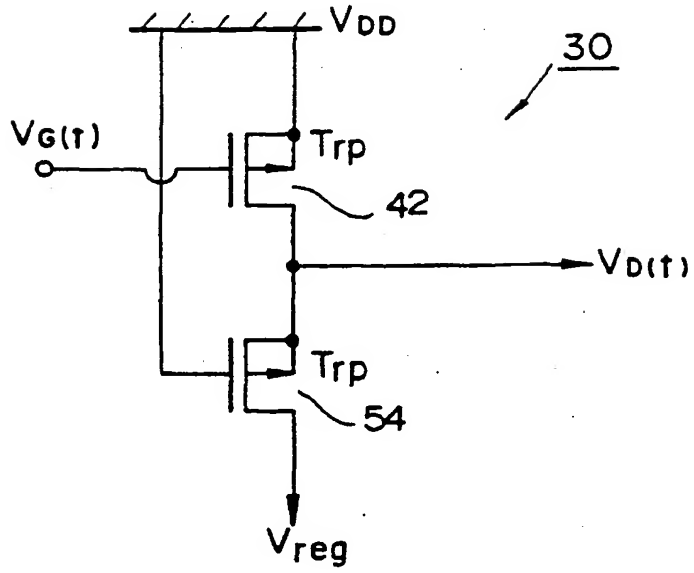
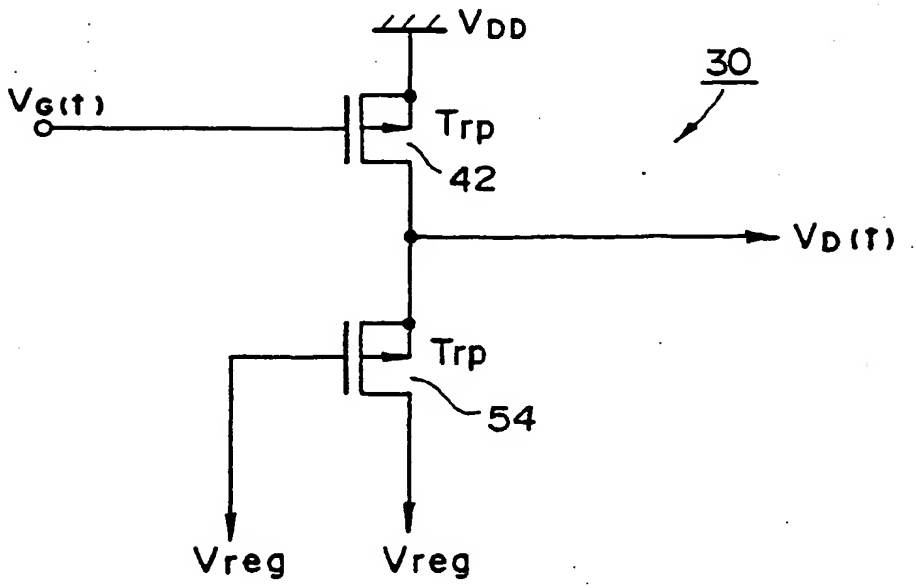


FIG. 17



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EUROPEAN SEARCH REPORT

Application Number
EP 97 12 2538

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	US 4 459 565 A (LEACH JERALD G) * column 5, line 57 - column 6, line 11; figures 1-5 *	1-11	G04F5/06 G04G1/00
Y	US 3 887 881 A (HOFFMANN KURT) * column 1, line 3 - column 2, line 2; figure 6 *	1-11	
A	US 4 352 073 A (LEUTHOLD OSKAR) * column 1, line 6 - column 3, line 41 *	1-11	
A	US 4 405 906 A (LUSCHER JAKOB) * column 1, line 6 - column 4, line 9 *	1-11	
A	US 4 095 195 A (SAITO TAKAHITO) * figures 1-9 *	1-11	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
G04F
G04G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 April 1998	Exelmans, U

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